UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,911	06/14/2005	David M. Fried	BUR20020072US1	5142

32074 7590 09/18/2007

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
WITHERS, GRANT S	

ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
09/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,911	FRIED ET AL.	
	Examiner	Art Unit	
	Grant S. Withers	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/28/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WALTER LINDSAY JR.
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the Amendment filed on 08/28/2007.

Currently, claims 1-18 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6-9, 11, and 13 are rejected under 35 U.S.C. 102(b) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996).

As to claim 1, Bryant discloses a method (See Figs. 6A-9) for forming a spacer (I-poly spacer 22; Fig. 8C; column 4, line 53) for a first structure (Gate poly 28 and sidewall portions of Cap Ox 30; Fig. 8C; column 4, line 64 and column 5, line 2) and a spacer for at most a portion of a second structure (Cap Ox 30 and the tip top of Gate poly 28; Fig. 8C; column 5, line 2, and column 4, line 64), the method comprising the steps of:

depositing a first material (poly of Gate poly 28; Fig. 8C; column 4, line 64);

forming a second material (oxide of Cap Ox layer 30; Fig. 8C; column 5, line 2) over the first material 28;

forming the first structure (Gate poly 28 and sidewall portions of Cap Ox 30; Fig. 8C; column 4, line 64, and column 5, line 2) from the first and second materials;

making the second material 30 overhang the first material 28; and

forming a spacer (I-poly spacer 22; Fig. 8C; column 4, line 53) under the overhang.

As to claim 2, Bryant further shows the method of claim 1, wherein the second structure (Cap Ox 30 and the tip top of Gate poly 28; Fig. 8C; column 5, line 2, and column 4, line 64) is made of monocrystalline silicon (all layers of polycrystalline silicon such as the tip top of Gate poly contain inherently portions of monocrystalline silicon), and the first material is made of polycrystalline silicon (Gate poly 28, Fig. 8C; column 4, line 64).

As to claim 3, Bryant further shows the method of claim 1, wherein the second material 30 is formed such that the second material has a faster oxidation rate (the oxide 30 would grow oxide faster than the lower portions of poly 28 far below it if the device subjected to oxygen since the poly far below it is surrounded by oxide and more poly than the upper portion of poly 28 feeding the oxide layer 30) the first material (lower parts of gate poly 28).

As to claim 6, Bryant further shows the method of claim 3, wherein the step of making includes oxidation (making oxide) to form the overhang as a result of a differential oxidation rate (oxide spacer film 32 deposited on cap ox 30 will grow faster than any oxide on the lower portion of gate poly 28) of the second

material with respect to the first material (Also, in the alternative, a slight oxide film will develop on Cap ox 30 faster than it will inherently grow on the lower portion of gate poly 28 in the ambient atmosphere of the processing chamber which will be oxidation occurring to form an overhang resulting from the difference in oxidation rates between the first and second materials).

As to claim 7, Bryant further shows the method of claim 3, wherein the step of making includes forming oxide on sides of the first structure and the second structure (portions of cap ox 30 formed on the sides of poly gate 28; Fig. 8C).

As to claim 8, Bryant further shows the method of claim 1 (with the alteration of referring to PSG layer 44 as "the second material"; Fig. 10C; column 5, line 33), wherein the second material 44 has different thermal reflow properties than the first material (Gate poly 28, Fig. 8C; column 4, line 64).

As to claim 9, Bryant further shows the method of claim 8, wherein the second material is one of BPSG and PSG (PSG layer 44; Fig. 10C; column 5, line 33).

As to claim 11, Bryant further shows the method of claim 1, wherein the step of forming the spacer 22 includes:

depositing a spacer material 22; and

directionally etching (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B; column 5, line 22) to form the spacer material 22 away except under the overhang.

As to claim 13, Bryant further shows the method of claim 1, wherein the first structure is a gate (gate poly 28 portion of the first structure in claim 1 above) and the second structure is a fin (a protruding portion of a mechanism resembling a fin) of a FinFET (The structure is a FET and it has a fin, broadly interpreted it is a finFET).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996), in further view of Bryant et al. (US 6,960,806, filed 06/21/2001).

As to claims 4 and 5, Bryant discloses the method cited above for claim 3.

However, regarding claim 4, Bryant fails to disclose a method as cited above for claim 3, wherein the second material includes a dopant including at least one of the group comprising: Arsenic, Germanium, Cesium, Argon, and Fluorine. Regarding claim 5, Bryant also fails to disclose a method as cited above for claim 3, wherein the second material is a deposited polycrystalline silicon-germanium alloy.

In the same field of endeavor, Bryant et al. show a method of forming a FinFET with a second material as part of the top portion of the gate made from

doped polysilicon (poly 218; Fig. 5; column 4, line 51) which can include Si-Ge (technology Si-Ge being used to make the poly gate; column 11, line 38) made using arsenic implants (n-FETs need to be implanted using arsenic; column 10, line 21).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of making an n-doped polysilicon-Ge for an upper layer of a gate as taught in Bryant et al. to have made the upper portion of the poly gate in Bryant with the motivation of using a material which has a greater number of carriers and a greater carrier mobility than ordinary polysilicon as used in Bryant (dopants increases the numbers of carriers, and SiGe's bandgap structure results in higher carrier mobility, See US 5,461,250, dated 08/10/1992, column 1, lines 50-51). The reasonable expectation for success results from the polysilicon-Ge gate structures as taught in Bryant et al. being well known in the art to form better gates for FET's such as in Bryant.

Regarding claim 14, Bryant discloses a method for forming a gate structure (Gate poly 28, Fig. 8C; column 4, line 64) and associated spacer (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B; column 5, line 22) for a FET, the method comprising the steps of:

depositing a first gate material (poly 28, Fig. 8C; column 4, line 64) over a portion of the FET;

forming a second material (top portion of Gate poly 28, Fig. 8C; column 4, line 64) over the gate material 28, wherein the second material 30 has a faster oxidation rate (the top portion of Gate poly 28 will grow oxide faster than the lower portions of the poly gate material due to increased exposure) than the gate material;

forming the gate structure (Gate poly 28, Fig. 8C; column 4, line 64) into (interpreted as being "from" as listed in objections) the gate material 28 and the second material 30;

oxidizing (growing oxide layer 32; Fig. 7C; column 5, line 10) to cause the second material 30 to overhang the gate material 28; and

forming a spacer (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B; column 5, line 22) under the overhang.

Regarding claim 15, Bryant discloses a method cited above for claim 14, wherein the gate material 28 is polycrystalline silicon (Gate poly 28, Fig. 8C; column 4, line 64).

Regarding claim 16, Bryant discloses a method cited above for claim 14, wherein the second material is a polycrystalline silicon (top portion of Gate poly 28, Fig. 8C; column 4, line 64) formed such that the second material has a faster oxidation rate than the first material (top portion of Gate poly 28 will oxidize faster than the lower portion due to increased exposure).

Regarding claim 17, Bryant discloses a method cited above for claim 14, wherein the step of oxidizing (forming oxide 32; Fig. 6B; column 5, lines 10-11) also forms oxide on sides of the gate 28.

Regarding claim 18, Bryant discloses a method cited above for claim 14, wherein the step of forming the spacer includes:

depositing a spacer material 22; and

etching (I-poly layer subjected to RIE to form spacers; Fig. 8B; column 5, lines 22-23) the spacer 22 material away except under the overhang.

Regarding claim 19, Bryant discloses a FET comprising;

a gate structure including an electrically conductive lower portion (Gate poly 28, Fig. 8C; column 4, line 64) and an overhanging top portion (Cap Ox 30; Fig. 8C; column 5, line 2);

a fin (Gate Ox 26; Fig. 8C; column 4, line 62); and

a spacer (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B; column 5, line 22) positioned under the top portion 30 of the gate structure adjacent to the lower portion 28.

Regarding claim 20, Bryant discloses a FET cited above for claim 19, wherein the top portion 30 is made of one of oxide (Cap Oxide 30; Fig. 8C; column 5, line 2) and (interpreted as "or" as in the objection above) glass, and the lower portion is made of polycrystalline silicon (Gate poly 28, Fig. 8C; column 4, line 64).

Regarding claim 21, Bryant discloses a FET cited above for claim 19, wherein the spacer 22 surrounds (partially surrounds by covering the top portion) the lower portion 28.

However, regarding claims 14-18, Bryant fails to disclose a method for forming a finFET wherein a monocrystalline fin extends through the lower portion, and has a spacer surrounding its fin, as opposed to a FET which lacks these features due to the nature of the particular design of FET illustrated.

In the same field of endeavor, Bryant et al. teach a method of forming a finFET wherein a monocrystalline fin (poly fin 218 including small portions of monocrystalline Si as all poly inherently does; Fig. 5; column 4, line 51) that has a spacer (spacer 244; Fig. 14; column 7, lines 29-30) partially surrounding its fin 218.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming a finFET wherein a fin that has a spacer partially surrounding its fin as taught by Bryant et al. to have formed the FET made in Bryant with the motivation of utilizing the standardized finFET design and gaining the benefits in terms of gate control that finFET gate wrapped around a channel offers.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996), in further view of Kunikiyo (US Pub. 2002/0135041, dated 09/26/2002).

As to claim 10, Bryant shows a method of forming an FET as cited above for claim 9.

However, Bryant fails to disclose a method wherein the method of forming an overhanging portion from a PSG containing material includes heating the material and causing it to reflow to form an overhanging portion.

In the same field of endeavor, Kunikiyo teaches a method of forming an overhanging (overhang; page 7, [0112], line 3) portion from a PSG (BPSG; page 7, [0112], line 1) containing material by heating the material and causing it to reflow (reflow; page 7, [0112], line 2).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming an overhang portion from BPSG as taught in Kunikiyo to have made the overhang portion in Bryant, with the motivation that BPSG should be used for overhang (BPSG should be used for overhang; page 7, [0112], line 3).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996), in further view of Wu et al. (US 6,770, 516, filed 09/05/2002).

As to claim 12, Bryant shows a method of forming an FET as cited above for claim 11.

However, Bryant fails to disclose a method wherein the spacer material is at least one of silicon nitride and (read as "or" as in objections above) silicon oxide.

In the same field of endeavor, Wu et al. teach a method of forming spacers (spacer 9; Fig. 5B; column 4, line 7) from silicon nitride (silicon nitride spacers 9; Fig. 5B; column 4, line 7).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming spacers out of silicon nitride as taught in Wu et al. to form the spacers in Bryant, with the motivation that in order to form N and P type source/drain regions in undoped portions of silicon shapes a silicon nitride spacer has to be employed (to form N and P type regions in silicon, a silicon nitride spacer has to be employed; columns 3 and 4, lines 66-67 and 1-3).

Response to Arguments

7. Applicant's corrections and arguments, see Amendment, filed 08/28/2007, with respect to the objections to the specification and drawings have been fully considered and are persuasive. The objections of the specification and drawings are withdrawn.

8. Applicant's arguments, see Amendment, filed 08/28/2007, with respect to the rejections under U.S.C 102 and 103 have been fully considered but they are not persuasive. The Applicant argues that the projecting part 30 in Bryant (US 5512517) is not to be considered an "overhang" when in fact, the very definition of the word "overhang" is "a projecting part" (American Heritage Dicitionary). The examiner takes the stance that the part 30 does indeed project away from other portions of itself. It is possible that a misunderstanding of the rejection might have arisen due to the Applicant assuming that one of ordinary skill in the art is limited to definitions of "overhang" such

as "to hang or be suspended over" (Dictionary.com), which perhaps may falsely lead to an implication that an overhanging object must not come into contact with an object it is overhanging. While it is permitted for the Applicant to act as his own lexicographer, the Applicant is reminded that it is not proper to redefine or narrowly restrict a word's ordinary meaning. Accordingly, the claims, 1, 6, etc. which involve the limitation "overhang" are not viewed by the examiner to limit these claims to portions which do not touch one another and while the claims are read in light of the specification it is improper to read limitations into the claims from an exemplary embodiment disclosed. It is also the examiners position that I-poly spacer is indeed formed "under the overhang" (See Fig. 7C), although it is not formed directly under the overhang, it would be improper to read such a limitation into a claim from the specification.

As to the inherency statement in claim 6, so far as the examiner is aware, known techniques of oxidizing silicon in a conformal fashion involve oxygen atoms near the surface of silicon as in Bryant. It is also known that even at ambient temperatures oxygen near the surface of silicon will form a thermal oxide layer. This effect may be controlled to acceptable levels in processes and depending on the dimensions of the device being created this effect may be more or less noticeable, but it will still occur, and there will be a difference in the oxidation rate of a poly layer and a silicon oxide layer resulting in a difference in the overall oxide layers created thereon. What is more, in this situation the discussion is involving a portion of the poly layer below the surface of the poly layer which one would be very hard pressed to oxidize at a rate anywhere near the oxidation rate of the existing silicon oxide. In any event, this is merely an

alternative way of viewing the situation, only to be considered if the first alternative should be overcome.

Bryant et al. is not relied upon to show an overhang, as one is already present in Bryant, and thus claims 4-5, and 14-21 stand rejected as in the prior Office Action.

Kunikiyo is not relied upon to show an overhang, as one is already present in Bryant, and thus claim 10 stands rejected as in the prior Office Action.

Wu et al. is not relied upon to show an overhang, as one is already present in Bryant, and thus claim 12 stands rejected as in the prior Office Action.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant S. Withers whose telephone number is 571-270-1570. The examiner can normally be reached on M-Th 7:30-5 (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GSW
09/04/2007

WALTER LINDSAY JR.
PRIMARY EXAMINER